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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/081,840	02/20/2002	Timothy A. Lewis	01-1016	3757

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LOREN H. MCROSS
PHOENIX TECHNOLOGIES LTD
915 MURPHY RANCH ROAD
MILPITAS, CA 95035

EXAMINER	
CLEARY, THOMAS J	

ART UNIT	PAPER NUMBER
2111	

DATE MAILED: 04/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/081,840	LEWIS, TIMOTHY A.	
	Examiner	Art Unit	
	Thomas J. Cleary	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 February 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 5 and 6 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claims 5 and 6 recite the limitations "repeats steps (3) and (4) until the predetermined bit of the read value is not set to zero" and "exits when the predetermined bit of the read value is not set to zero". The specification describes performing these actions when the predetermined bit is set to zero, not when the predetermined bit is not set to zero.

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1-2, and 4-6 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

5. Claims 1 and 2 recite the limitation "a status latch for storing the status of the timer" in Line 15 of Claim 1. It is unclear if the timer referred to is the "retriggerable fixed duration timer" or the "timer that is triggerable by reading zero from the first register location".

6. In reference to Claims 5 and 6, since the predetermined bit can only exist in one of two states (set or not set), it is unclear as to how one action can be performed if the bit is set, and another action can be performed if the bit is not set to zero. A bit which is set and a bit which is not set to zero are in the same state.

7. In reference to Claims 2, 4, and 6, it is unclear which bit is bit 7. The Examiner is unclear as to whether the bits are numbered 7-6-5-4-3-2-1-0 (big endian notation) or 0-1-2-3-4-5-6-7 (little endian notation).

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 3-6 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent Number 5,684,997 to Kau et al. ("Kau").

10. In reference to Claim 3, Kau discloses a method for improving system management interrupt (SMI) latency of a system comprising the steps of: reading a status latch (See Column 132 Line 58); stopping if the value read from the status latch is zero (See Column 132 Line 58); writing to a first I/O location (See Column 132 Lines 29-32); reading a second I/O location (See Column 132 Lines 29-32); and if a predetermined bit of the value that is read from the second I/O location is set, repeating the writing and reading steps until the predetermined bit of the read value is not set (See Column 133 Lines 11-15 and 20-23).

11. In reference to Claim 4, Kau discloses the limitations as applied to Claim 3 above. Kau further discloses writing 0A to I/O location 0x70, which is the first I/O location (See Column 132 Lines 29-32, Column 132 Lines 51-57, and Column 133 Lines 20-23), reading I/O location 0x71, which is the second I/O location (See Column 132 Lines 29-32, Column 132 Lines 51-57, and Column 133 Lines 20-23), and if bit 7 of the value read from I/O location 0x71 is set, repeating the previous two steps until the value of bit 7 is not set, and then stops (See Column 133 Lines 11-15 and 20-23).

12. In reference to Claim 5, Kau discloses a method for improving system management interrupt (SMI) latency of a system having timing-sensitive registers, a status latch, and a plurality of I/O locations, comprising: (1) a code segment that reads a status latch (See Column 132 Line 58); (2) a code segment that stops if the value read from the status latch is zero (See Column 132 Line 58); (3) a code segment that writes to a first I/O location (See Column 132 Lines 29-32); (4) a code segment that reads from a second I/O location (See Column 132 Lines 29-32); (5) a code segment that, if a predetermined bit of the second value that is read from the second I/O location is set, repeats steps (3) and (4) until the predetermined bit of the read value is not set (See Column 133 Lines 11-15 and 20-23); and (6) a code segment that exits when the predetermined bit of the read value is not set (See Column 133 Lines 11-15 and 20-23).

13. In reference to Claim 6, Kau discloses the limitations as applied to Claim 5 above. Kau further discloses writing 0A to I/O location 0x70, which is the first I/O location (See Column 132 Lines 29-32, Column 132 Lines 51-57, and Column 133 Lines 20-23), reading I/O location 0x71, which is the second I/O location (See Column 132 Lines 29-32, Column 132 Lines 51-57, and Column 133 Lines 20-23), and if bit 7 of the value read from I/O location 0x71 is set, repeating the previous two steps until the value of bit 7 is not set, and then stops (See Column 133 Lines 11-15 and 20-23).

Duty to Disclose

14. Applicant is reminded that each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in 37 CFR 1.56. Applicant is advised to submit any information material to patentability in accordance with 37 CFR 1.97 and 1.98.

Response to Arguments

15. Applicant's arguments, see Pages 8-13, filed 10 February 2005, with respect to the rejection(s)of Claim(s) 1-6 under 35 USC § 103 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of a different interpretation of the previously applied art.

Conclusion

16. The following prior art made of record and not relied upon is considered pertinent to Applicant's disclosure: US Patent Number 6,694,445 to Leidich; US Patent Number 5,678,019 to Podkowa et al.; US Patent Number 4,742,475 to Keiser et al.; US Patent

Number 4,303,850 to Juhosz et al.; "Using the RTC" by Jan Verhoeven; "App Note 2740: Accessing the DS1318 Clock Registers" by Dallas Semiconductor.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas J. Cleary whose telephone number is 571-272-3624. The examiner can normally be reached on Monday-Thursday (7-3:30), Alt. Fridays (7-2:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H. Rinehart can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TJC

Thomas J. Cleary
Patent Examiner
Art Unit 2111